ABSTRACT

An embedded DRAM ECC architecture for purging data errors is disclosed. The embedded DRAM ECC architecture is based upon a two-dimensional linear parity scheme, and includes a plurality of memory blocks and a parity block. Each memory block includes additional columns for storing row parity bits, and the parity block stores column parity bits. A row parity circuit coupled in parallel to an existing local databus of each memory checks the parity of the local databus bits against a row parity bit during a refresh or read operation in order to identify parity failure for the word. Identification of the incorrect bit of the word is achieved by iteratively transferring the data of the local databus of each memory block onto an existing global databus, and checking the parity across the global databus with a column parity circuit. When global databus parity failure is detected, all bits of the global databus are inverted to purge the incorrect bit from the memory block via the local databus. A method for initializing the memory upon power up in order to prepare the memory for writing data, and methods and circuits for generating the corresponding row and column parity bits during a write operation are also disclosed.